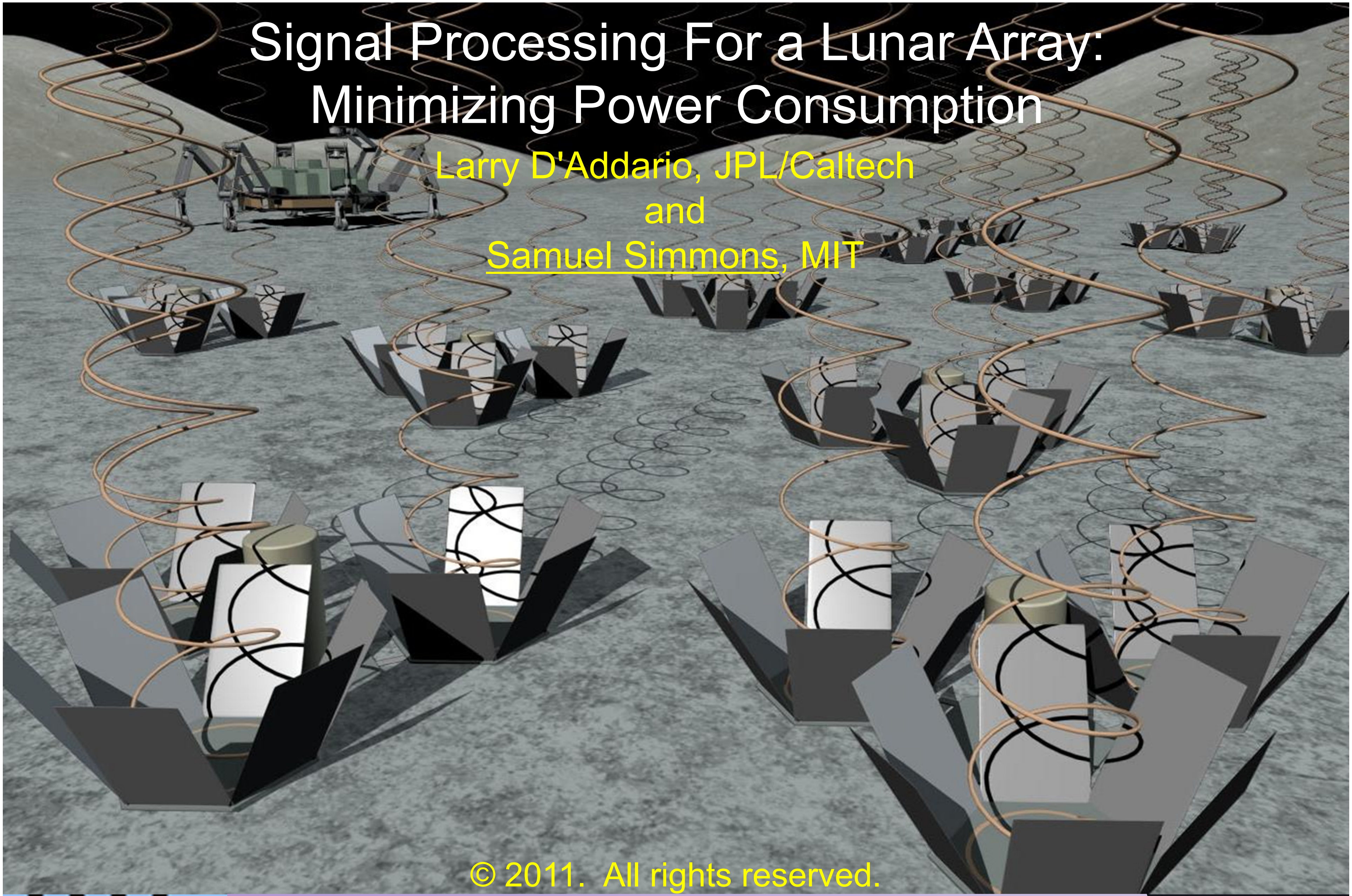

Signal Processing For a Lunar Array: Minimizing Power Consumption

Larry D'Addario, JPL/Caltech
and
Samuel Simmons, MIT

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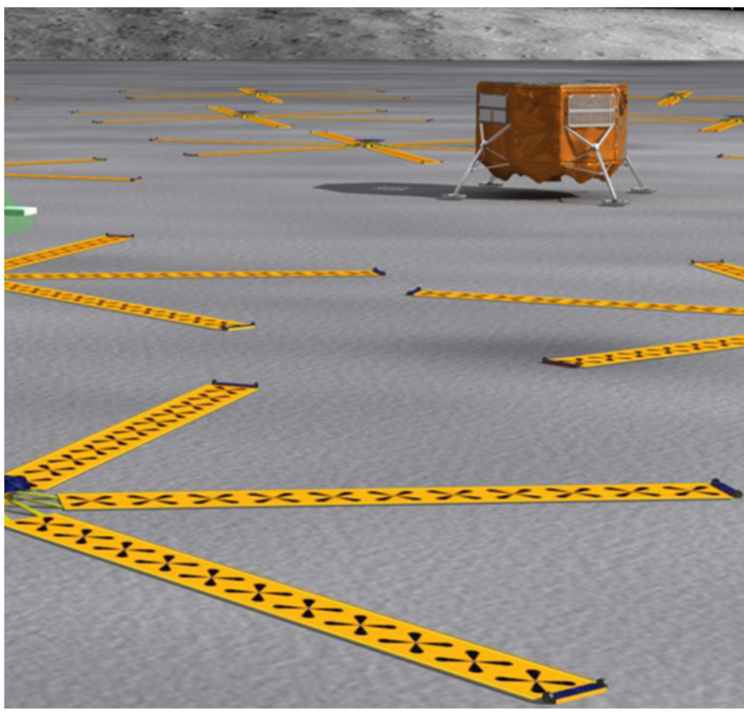
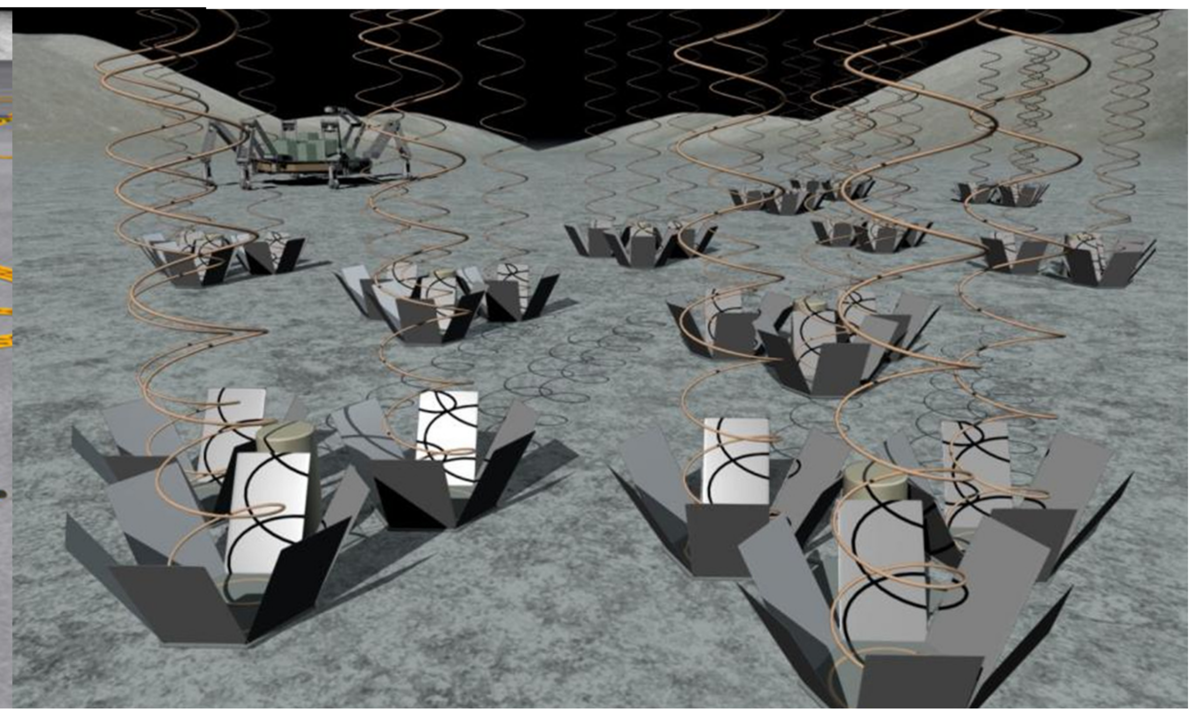
Background (1 of 2)

- Motivation
  - Lunar Radio Array for low frequency, high redshift Dark Ages/Epoch of Reionization observations (z=6-50, f=30-200 MHz)
  - High precision cosmological measurements of 21 cm H I line fluctuations
  - Probe universe before first star formation and provide information about the Intergalactic Medium and evolution of large scale structures
  - Does the current cosmological model accurately describe the Universe before reionization?
- Lunar Radio Array
  - Radio interferometer based on the far side of the moon
    - Necessary for precision measurements
    - Shielding from earth-based and solar RFI
    - No permanent ionosphere
  - Minimum collecting area of ~1 km^2 and brightness sensitivity 10 mK
  - Several technologies must be developed before deployment

Background (2 of 2)

- Two different concepts have been proposed
- Dark Ages Radio Interferometer (DALI)
  - 300 stations each consisting of 1500 printed dipole elements
  - Multiple beams are formed at each station
  - All pairs of stations are cross-correlated, separately for each beam
- Lunar Array for Radio Cosmology (LARC)
  - 10,000-20,000 elements each consisting of four helical antennas
  - All pairs of elements are cross-correlated

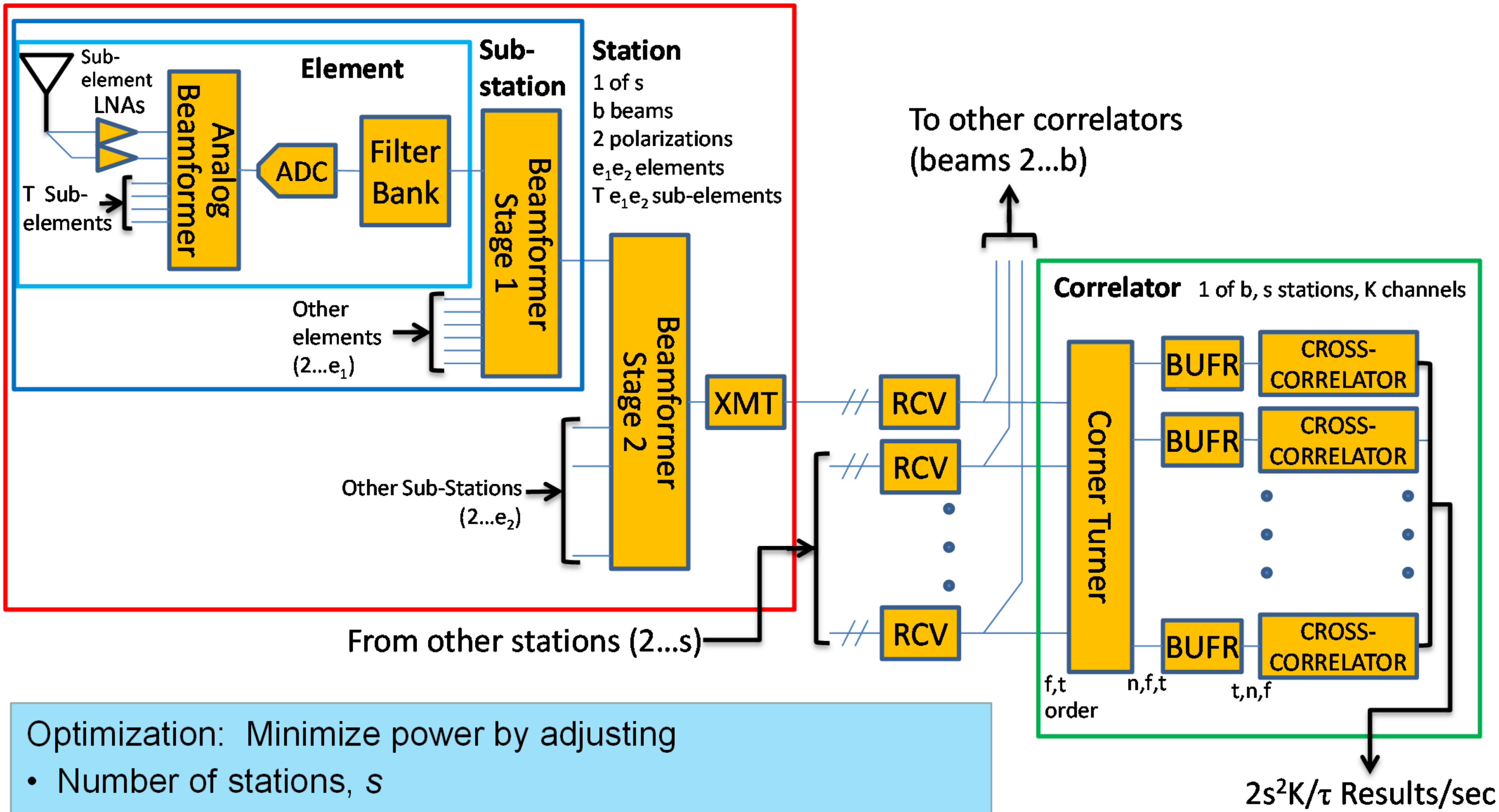




Summary of Results

- Approach
  - Consider all signal processing elements from antennas through correlator
  - Model the power dissipation of each element using available data
  - Optimize the design so as to minimize the total power dissipation, keeping survey speed constant, subject to some constraints
- Findings
  - FFT telescope, MOFF correlator, Omniscope: rejected as impractical.
  - Power tradeoff favors clustering antennas into relatively few stations, each with many elementary antennas formed into multiple beams.
  - Beamforming is best done with two hierarchical stages
  - Cross-correlation is best done with a separate multiply-accumulator for each baseline so as to avoid power-hungry memory operations. This leads to a matrix (not pipeline) architecture.
  - In the optimized design, power use is dominated by LNAs and signal transmission. Cross correlation uses only about 10%.
  - In current technology, A_{eff} = 0.5 km^2 with FoV = 1000 deg^2 at zenith can be achieved using <20kW for all processing from antennas through correlator.

Selected Architecture – Block Diagram



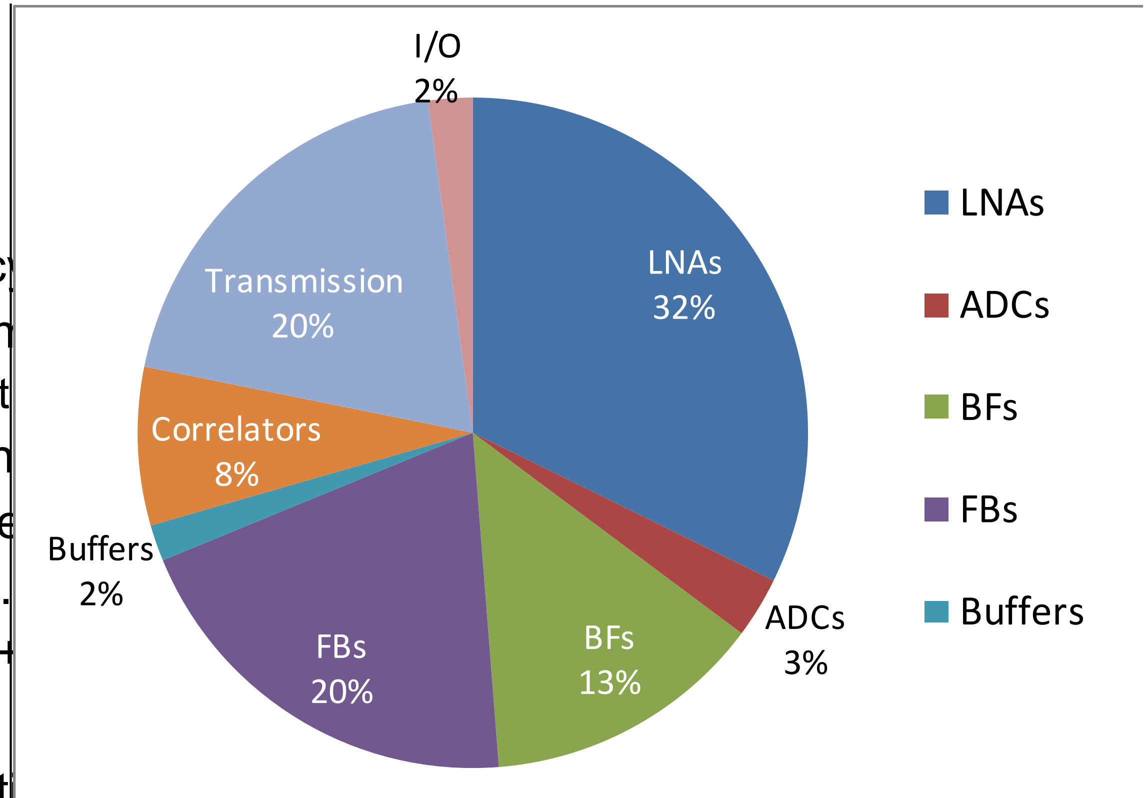
Optimization: Minimize power by adjusting

- Number of stations, s
- Number of beams, b

while keeping survey speed $S = A^2\Omega$ constant, producing

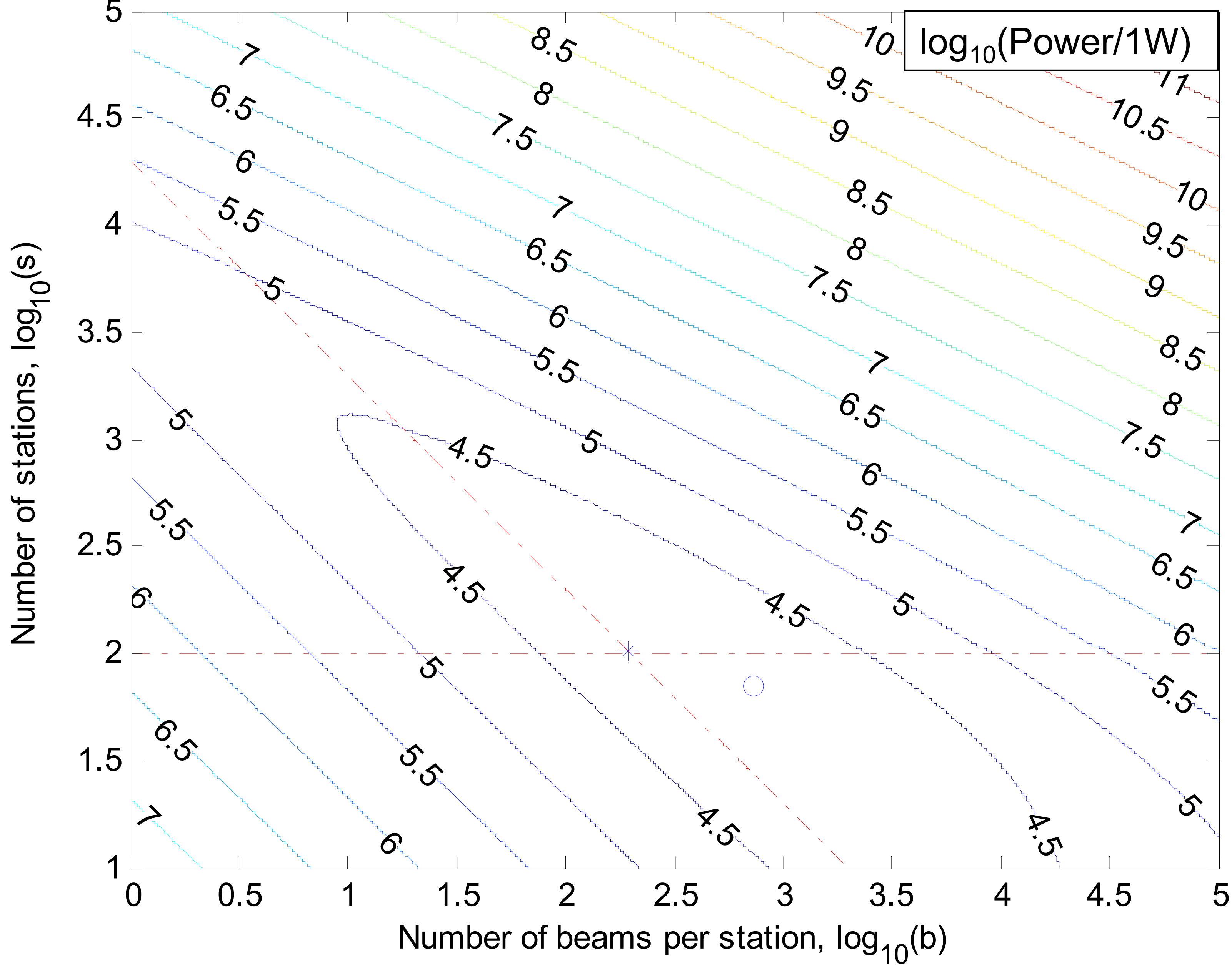
- Total effective area $A = e\eta A_e$ for e antenna elements
- Total field of view $\Omega = b\Omega_s$ for station beam size Ω_s .

Parameters



- Fixed
  - 90 MHz center frequenc
  - Quad-helix antenna elen
    - Effective area 39 m^2 at
  - 170 MHz processed ban
  - 16384 frequency channe
  - Survey speed $A^2\Omega$ = 1.
  - Sample quantization 2b+
- Constraints
  - Minimum number of stati
  - All station beams must fit inside element beam
- Results
  - 104 stations with 240 elements each
  - 192 beams formed at each station, filling the element beam
  - Total signal processing power 18.6 kW
- Not included
  - Support circuits like voltage converters
  - Monitor and control

Minimization of Power at Constant Survey Speed



Power Consumption Models

$$P = 2e(Tc_{e1} + Bc_{e2})$$

$$+B[2c_{bf}b\sqrt{es} + c_f e \log_2 K + 2c_m bs + c_c bs(2s+1) + 2c_t bs + c_i p]$$

All values scaled to 90 nm CMOS technology, 2b+2b sample size.

Sym	*Parameter*	*Value*	*Units*	*Basis*
c_{e1}	power per LNA (indep of bandwidth)	0.03	W	optimistic guess
c_{e2}	energy per sample digitized (ADC)	1.33E-10	J	published 5 GSa/s 6b ADC, scaled [1]
c_f	energy per Filter Bank operation (FFT radix 2 butterfly)	6.26E-11	J	published spectrometer ASIC [2]
c_c	energy per CMAC operation	2.00E-12	J	ALMA, EVLA, GeoStar chips scaled
c_{bf}	energy per frequency-domain beamformer operation	1.20E-11	J	analogy to CMAC; coefficients in RAM
c_{bt}	energy per time-domain beamformer operation	8.00E-11	J	analogy to CMAC, length 18 FIR interpolator
c_i	energy per I/O (one sample, chip to chip)	1.23E-11	J	published high-speed transceiver ASIC [3]
c_t	energy per transmission (one sample, station to center)	5.40E-10	J	COTS optical link [4]
c_m	energy per Read+Write to RAM (one sample)	4.80E-11	J	COTS DRAM [5]

[1] M. Choi et al., "A 6-bit 5-GSample/s Nyquist A/D converter in 65nm CMOS," 2008 IEEE Symp. on VLSI Circuits.

[2] B. Richards et al., , "A 1.5GS/s 4096-Point Digital Spectrum Analyzer for Space-Borne Applications." IEEE Custom Integrated Circuits Conference, September, 2009.

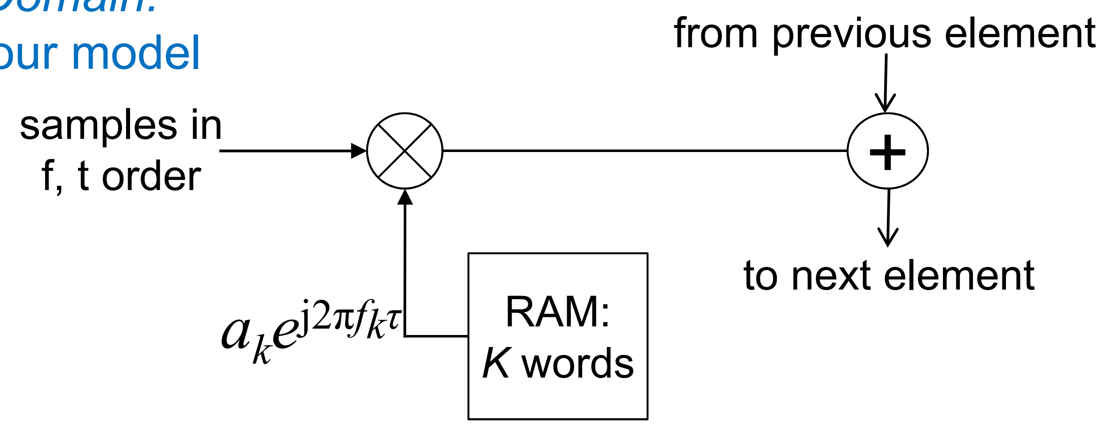
[3] P. Palmer et al., "A 14mW 6.25Gb/s Transceiver in 90nm CMOS for Serial Chip-to-Chip Communications." IEEE Solid State Circuits Conference, 2007.

[4] Advanced Optronice Devices, model AODM-XT154-LD-CD-MF data sheet.

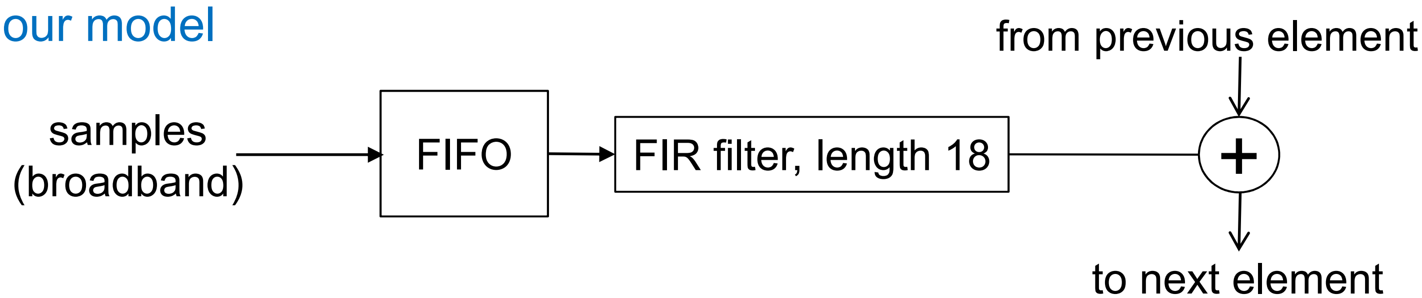
[5] Hynix PN H5TC1G83TFR-H9A, 128Mx8 SDRAM, data sheet.

Beamformers –Time Domain vs. Frequency Domain

Frequency Domain:
12 pJ/op in our model



Time Domain:
80 pJ/op in our model



Both cases:
To form *b* beams from *e* antenna signals requires

- *be* of these beamforming elements if done in 1 stage
- 2*b* sqrt(*e*) of these beamforming elements if done in 2 stages

"What If?" Questions

- Minimum number of stations is constrained to be larger?
  - perhaps necessary for adequate uv-plane coverage
- Processed bandwidth is reduced?
  - practical antenna elements are efficient over < 1 octave
- Required survey speed is reduced? or increased?
- Dipoles are used as antenna elements rather than quad helixes?
- Original LARC concept is used?
  - all elements separately correlated, not aggregated into stations
- Original DALI concept is used?
  - 300 stations with 1500 dipoles each.

"What If?" Answers

	S m^4	B MHz	s_{min}	stations	beams	elements	power W
Original DALI concept [1]	1.74E+11	170	100	300	52	450,000	82,216
Original LARC concept [2]	1.75E+11	170	100	20,000	1	20,000	300,030
Dipoles, optimized	1.74E+11	170	100	159	401	110,097	60,614
Quad helixes, optimized	1.74E+11	170	100	104	192	24,964	18,567
reduced bandwidth	1.74E+11	50	100	104	192	24,964	9,690
reduced survey speed	4.35E+10	170	100	100	99	12,490	8,907
increased min. stations	1.74E+11	170	300	300	66	24,964	20,356

[1] Number of beams was not specified; chosen here to produce specified survey speed.

[2] Survey speed produced by given number of single-beam elements.

Discussion

- Why are our power estimates so low?
  - We assume ASICs for FBs, BFs, and correlators – not GPUs nor FPGAs
  - We assume current technology (90 nm CMOS)
    - not 250 nm (ALMA) nor 130 nm (EVLA)
    - but we're not pushing technology (45 nm is available now, but expensive) and we're not invoking Moore's Law.
  - We use a power-efficient correlation architecture
    - Each baseline gets a dedicated CMAC, minimizing buffering and interconnections.
    - Results in more chips at slower clock speed (22 MHz), but far less power.
- Why do compound antennas (quad helixes) result in less power than dipoles?
  - The compound antennas accomplish part of the beamforming for "free" with passive components that use no power
  - Quad helix beam is 0.28 sterradians, vs. about 4 sterradians for a dipole
  - Although they use less processing power, the compound antennas are more complex and have more mass per unit collecting area.

Conclusions and Disclaimers

- The power needed to process signals from a large array of non-steerable elements is not prohibitive, even for the Moon, and even in current technology.
- The power required will be less in future technologies.
  - Smaller gate length CMOS is clearly foreseeable.
  - Substantially different semiconductor materials and transistor types may produce additional power reduction.
- The tall pole in power consumption seems to be LNAs, not digital electronics.
- Similar results apply to arrays on Earth with similar parameters.
  - SKA-low, HERA
  - But additional design constraints may be needed to ensure that ionospheric effects can be corrected.
- Our analysis neglects support circuitry (power supplies and M/C)
  - We guess that about 30% more power will be needed for these
- Our analysis is based on scaling existing designs, modeling, and data sheets
  - No detailed design has been done, so accuracy of our results is uncertain.

Acknowledgments

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